MAY 26 2006
PATENT & TRADEMARK OFFICE


```
ENTITY FSM IS

    PORT(
            ....ports for entity fsm....
        );

    ARCHITECTURE FSM OF FSM IS

    BEGIN

            ... HDL code for FSM and rest of the entity ...

            fsm_state(0 to 2) <= ... Signal 801 ...

    853 --!! Embedded FSM : examplefsm;
    859 --!! clock        : (fsm_clock);
    854 --!! state_vector : (fsm_state(0 to 2));
    855 --!! states       : (S0, S1, S2, S3, S4);
    856 --!! state_encoding : ('000', '001', '010', '011', '100');
        --!! arcs         : (S0 => S0, S0 => S1, S0 => S2,
    857 --!!               (S1 => S2, S1 => S3, S2 => S2,
        --!!               (S2 => S3, S3 => S4, S4 => S0);
    858 --!! End FSM;

                ,
                ,
                ,
                ,
                ,
                ,
                ,

END;
```

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Fig. 8C
Prior Art

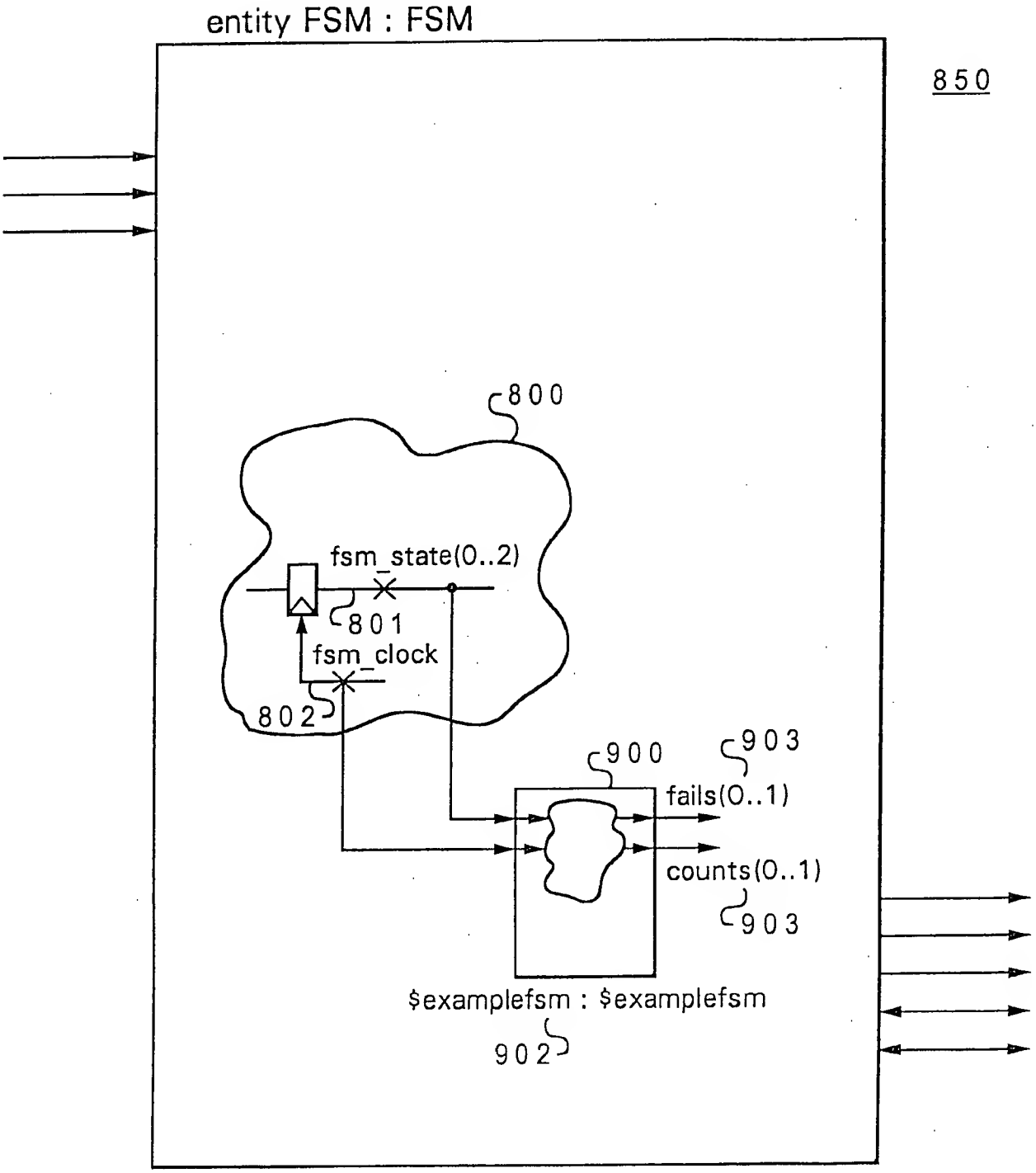

Fig. 9
Prior Art

Fig. 10A Prior Art

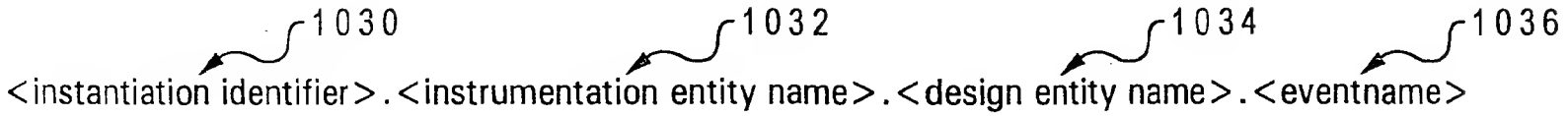

Fig. 10B

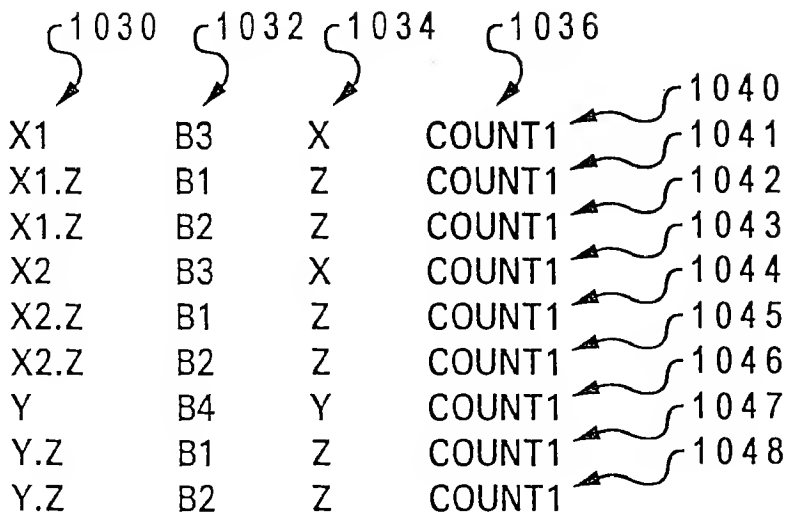

Fig. 10C

Fig. 10D
Prior Art

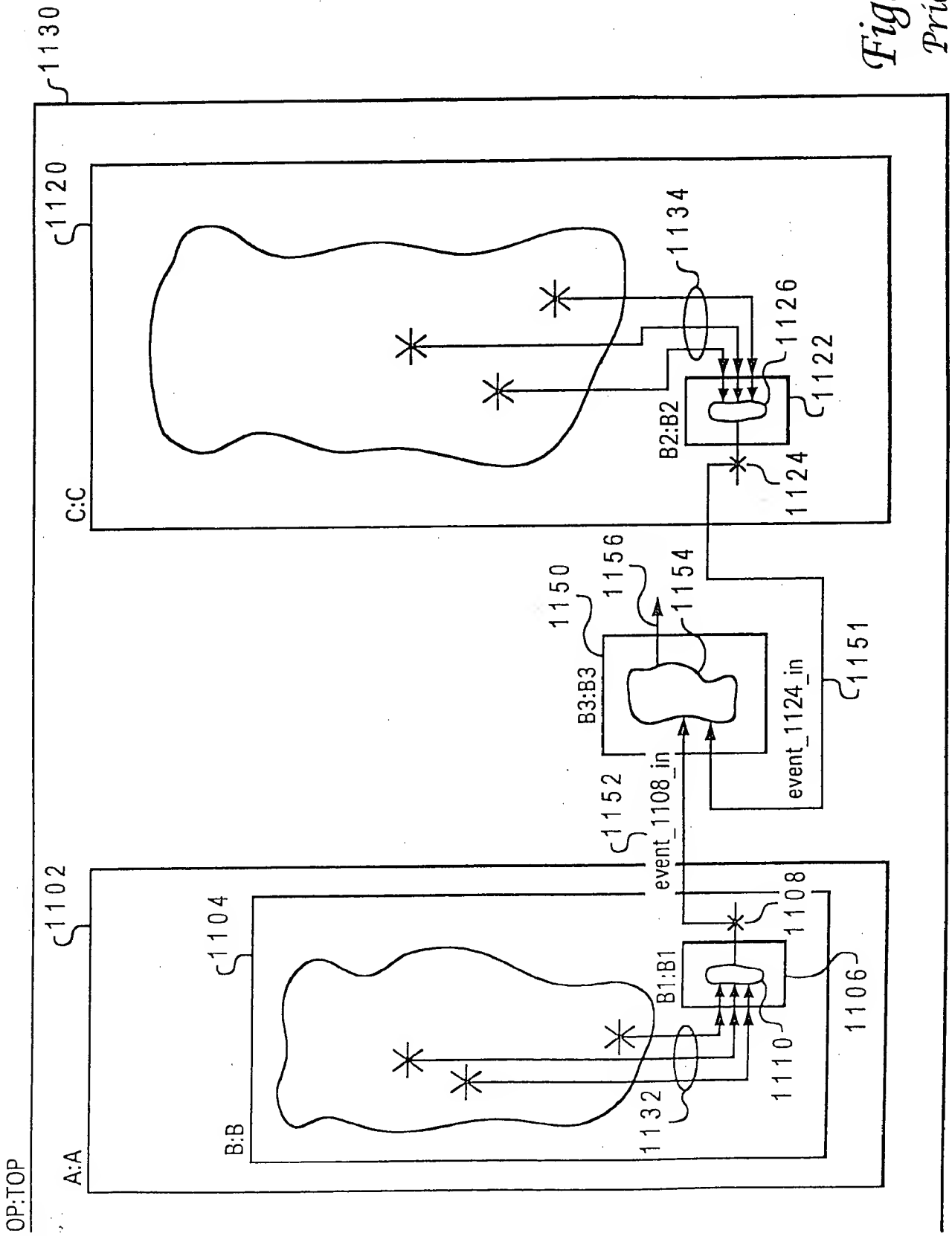

Fig. 11A
Prior Art

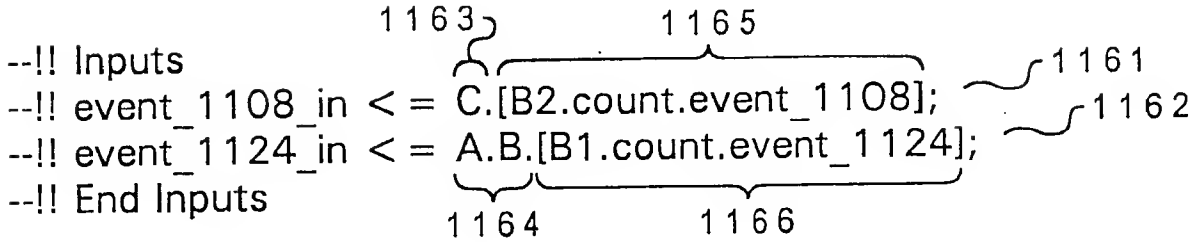

Fig. 11B

```
--!! Inputs
--!! event_1108_in <= C.[count.event_1108];
--!! event_1124_in <= B.[count.event_1124];
--!! End Inputs
```

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Fig. 11C
Prior Art

AUS920000651US1
Gabele, et al.
Non-Redundant Collection Of Harvest Events
Within A Batch Simulation Farm Network

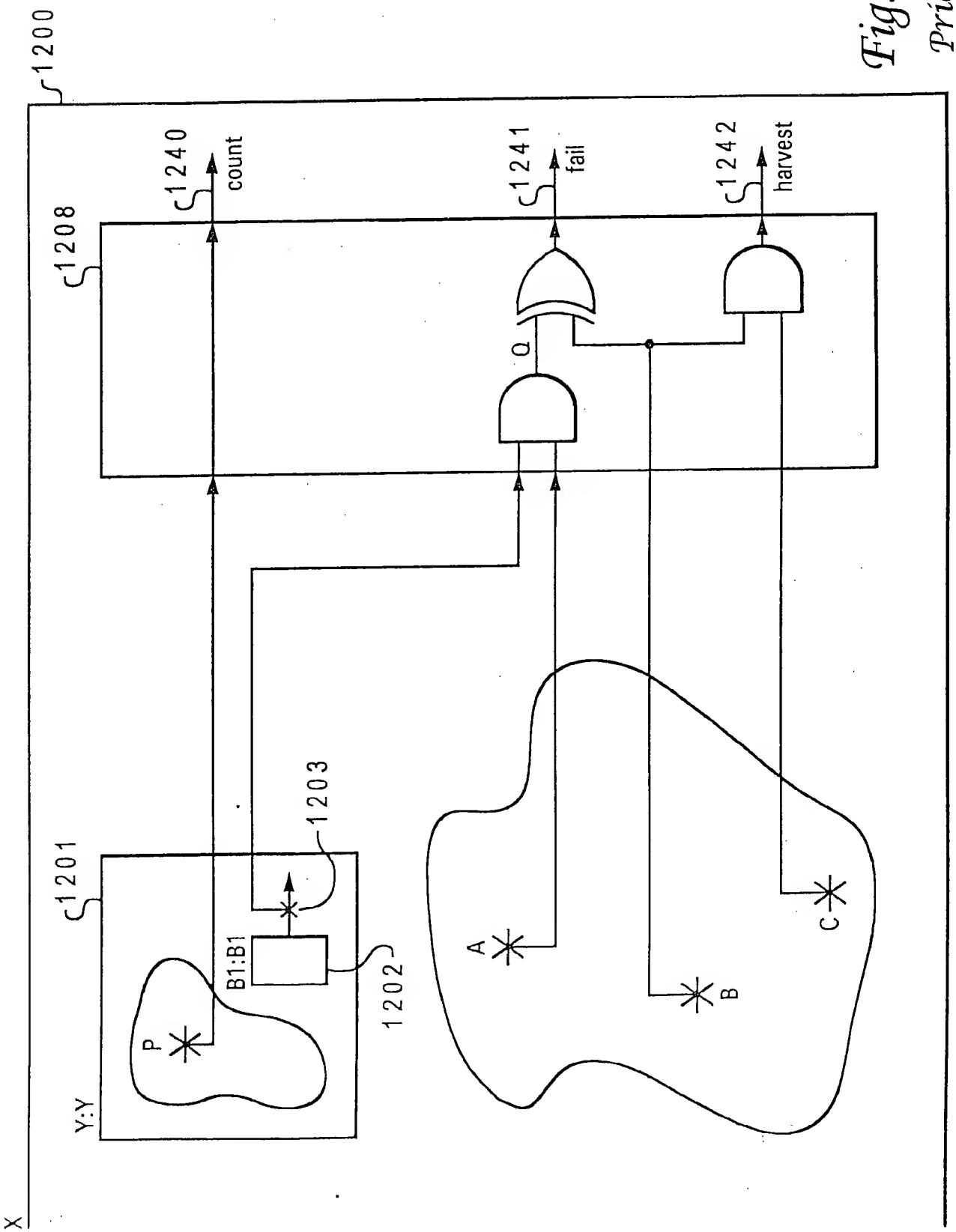

Fig. 12A
Prior Art

```
ENTITY X IS

    PORT(    :
             :
             :
         );

ARCHITECTURE example of X IS

BEGIN
    .
    .
    .
    .
    .
  ... HDL code for X ...
    .
    .
    .
    .
    .

    Y:Y
    PORT MAP(    :
                 :
             );

    A <= ....
    B <= ....
    C <= ....

    --!! [count, countname0, clock] <= Y.P;
    --!! Q <= Y. [B1.count.count1] AND A;
    --!! [fail, failname0, "fail msg"] <= Q XOR B;
    --!! [harvest, harvestname0, "harvest msg"] <= B AND C;

END;
```

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1234

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Fig. 12B
Prior Art

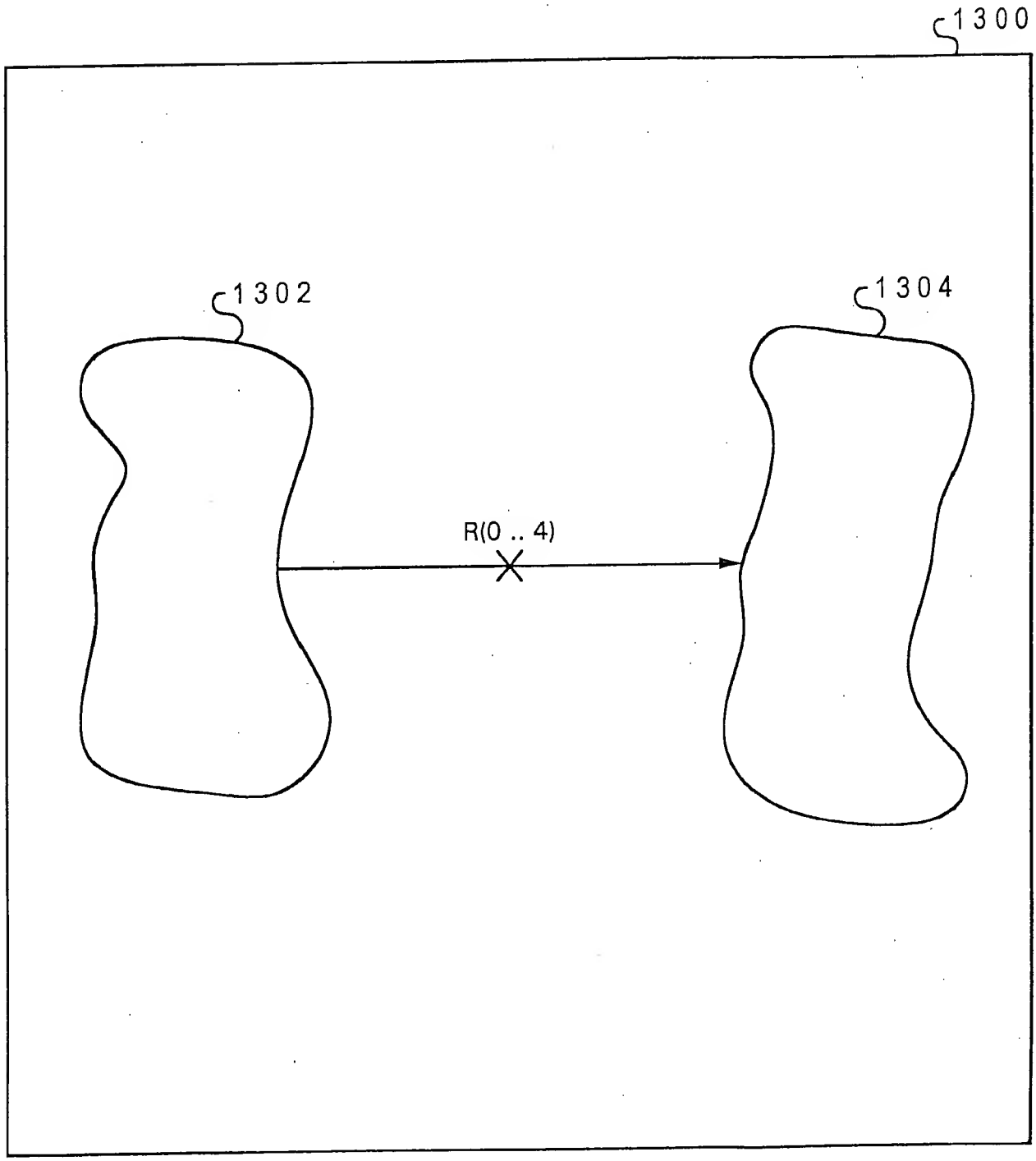

Fig. 13A
Prior Art

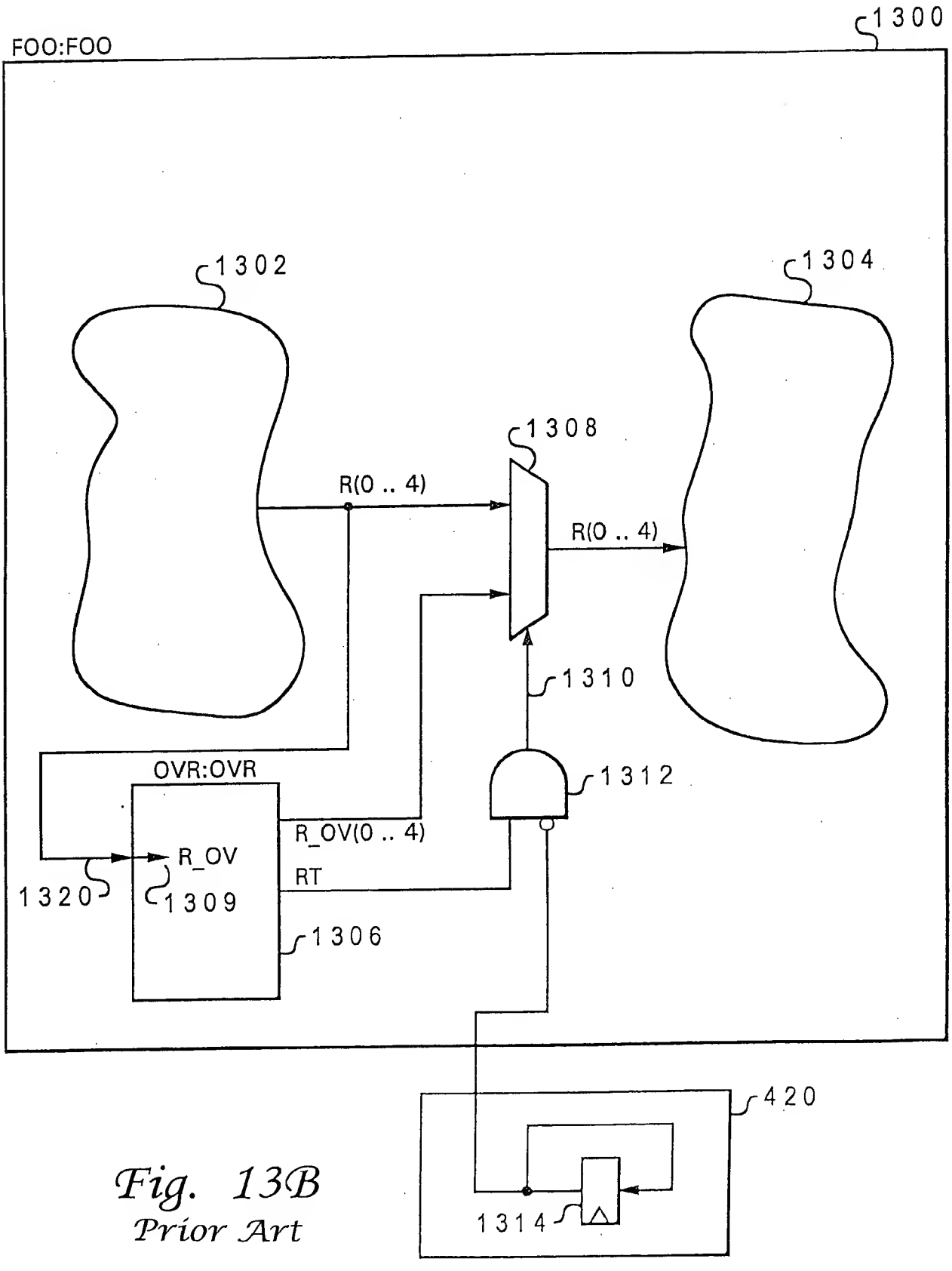

Fig. 13B
Prior Art

```
ENTITY OVR IS                                          1364
     PORT(   R_IN        :     IN std_ulogic_vector(0 .. 4);
                .
                .
                .
             ... other ports as required ...
                .
                .                                          1362
                .
             R_OV        :     OUT std_ulogic_vector(0 .. 4);
             RT          :     OUT std_ulogic
          );                                    1363
--!! BEGIN
--!! Design Entity: FOO;

--!! Inputs (0 to 4)                    1360
--!! R_IN => {R(0 .. 4)};
--!! :
... other ports as needed ...
--!! :
--!! End Inputs
                                   1361
--!! Outputs
--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS

BEGIN

     ... HDL code for entity body section ...

END;
```

1356 — 1351 — 1340 — 1358

Fig. 13C
Prior Art

```
ENTITY FOO IS

    PORT(    :
             :
             :
        );

ARCHITECTURE example of FOO IS

BEGIN

    .
    .
    .
    .
    .
    R <= ......
    .
    .
    .
    .
    .                    1381
    --!! R_IN <= {R};
    --!!                      1382
    --!!
    --!! R_OV(0 to 4) <= ......;        1383
    --!! RT <= ......;
    --!! [override, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
                                 1384
```

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Fig. 13D
Prior Art

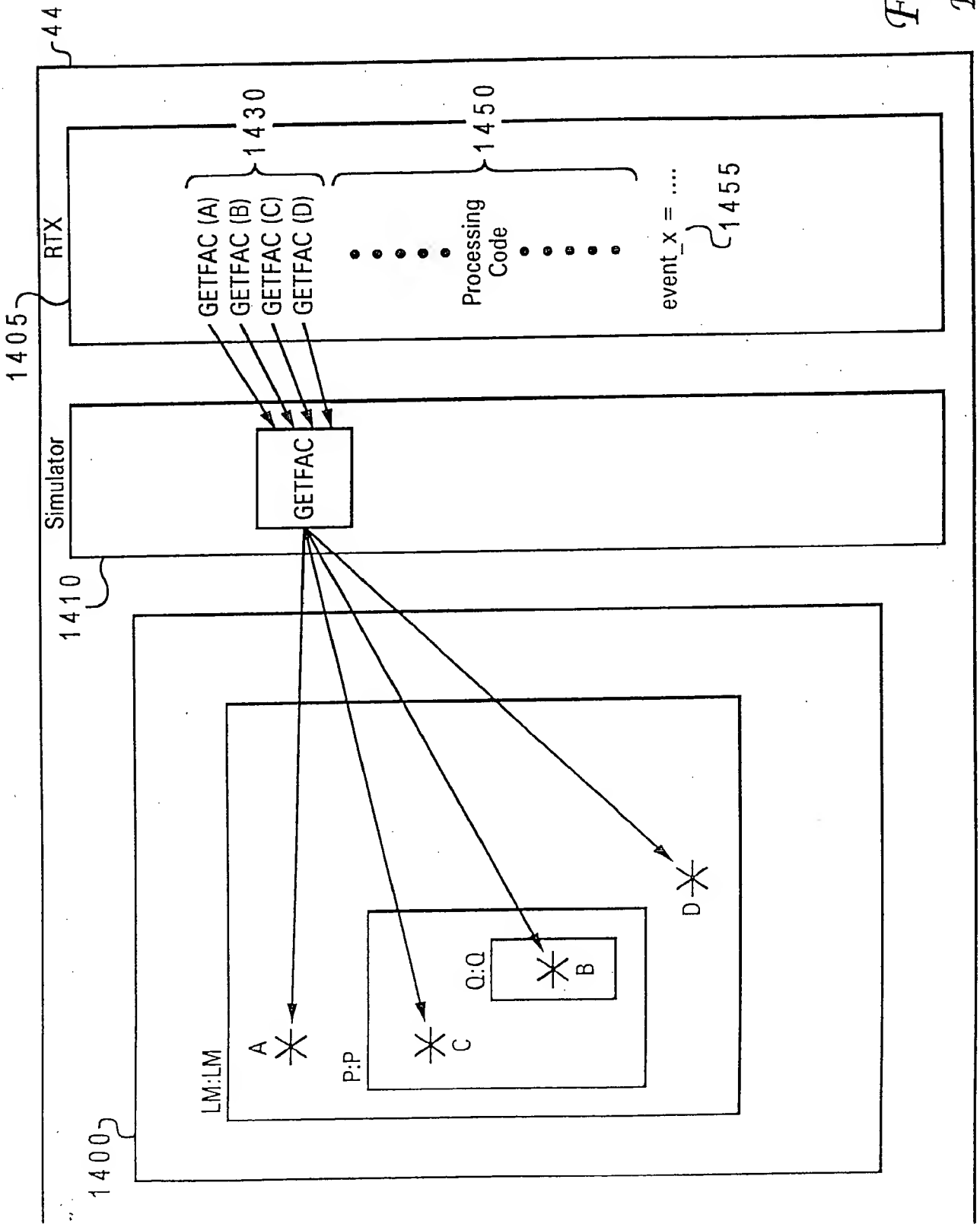

Fig. 14A
Prior Art

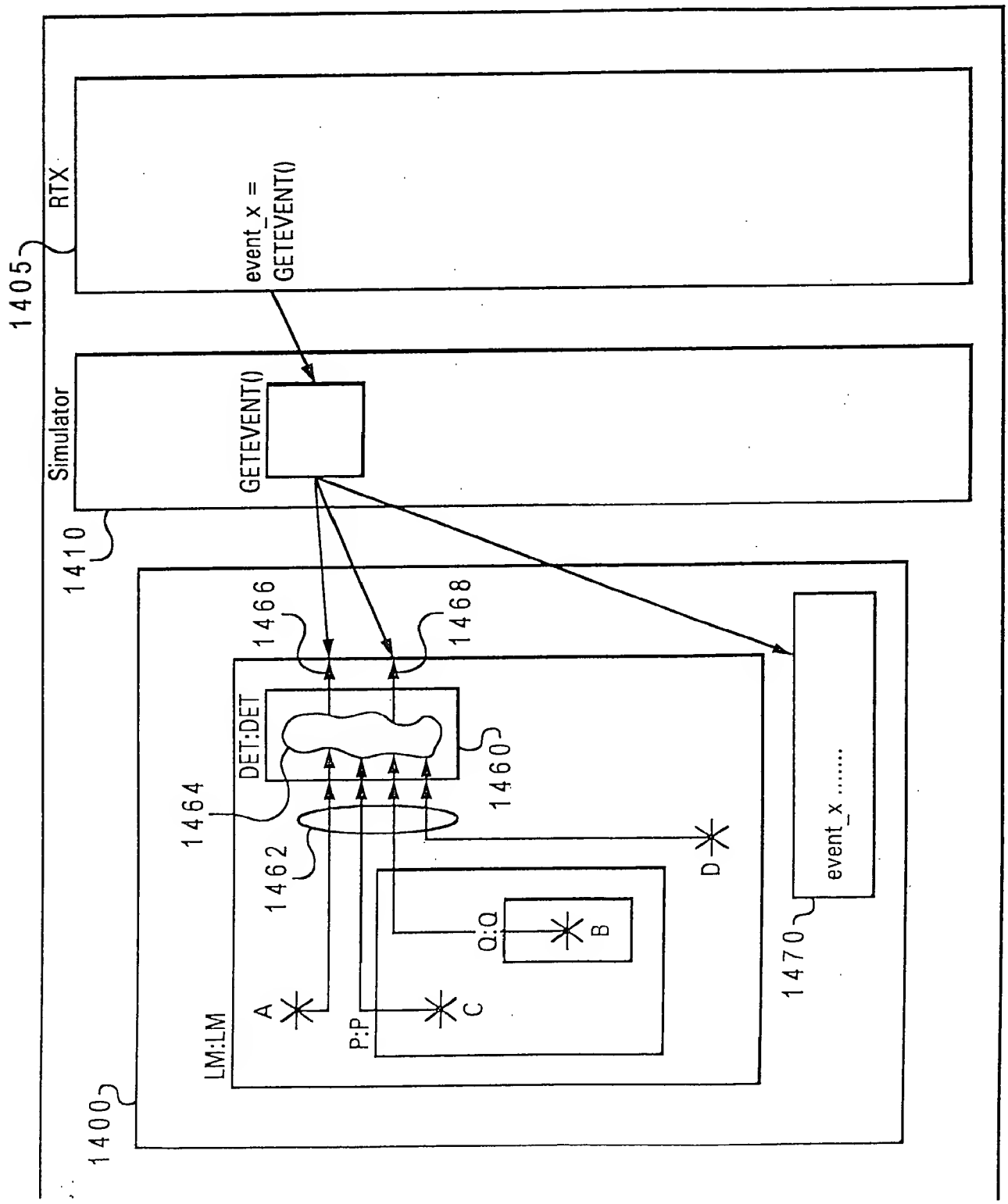

Fig. 14B
Prior Art

```
ENTITY DET IS

    PORT(   A           :   IN std_ulogic;
            B           :   IN std_ulogic_vector(0 to 5);
            C           :   IN std_ulogic;
            D           :   IN std_ulogic;
                        :
                        :
            event_x     :   OUT std_ulogic_vector(0 to 2);
            x_here      :   OUT std_ulogic;
        );

--!! BEGIN
--!! Design Entity: LM;

--!! Inputs
--!! A     =>    A;
--!! B     =>    P.Q.B;
--!! C     =>    P.C;
--!! D     =>    D;
--!! End Inputs

--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections

--!! End;

ARCHITECTURE example of DET IS

BEGIN

    ... HDL code ...

END;
```

1491 1492 1493 1494 1495 1480

Fig. 14C
Prior Art